SYNOPSYS®

DATASHEET

TestMAX Advisor

Address Testability Issues Early

Design-for-test rule checking and RTL fault coverage estimation capabilities that help designers pinpoint testability issues early in the flow

Overview

Synopsys TestMAX™ Advisor, performs RTL testability analysis and optimization, allowing users to fine-tune RTL early in the design cycle to predictably meet manufacturing and in-system test coverage goals. Advisor is commonly used throughout the design implementation flow at various handoff points when the designs content changes.

Advisor checks for testability issues in advance, checking how suitable the RTL or NetList is for test and checks to see if it is ready for DFT logic insertion. Advisor also performs analysis to determine where to place these DFT structures called test points that can improve the results of ATPG or Logic BIST.

Advisor is built on Synopsys SpyGlass® technology and provides a comprehensive set of early RTL testability analysis capabilities as well as allows the traditional netlist-based flow.

Key Benefits:

- Shortens test implementation time and cost by ensuring RTL or netlist is scan-compliant
- Improves test quality by diagnosing DFT issues early at RTL or netlist
- Detects source of static and dynamic X Capture and provides impact analysis
- Reduce ATPG pattern counts and run times and improve coverage
- Systematically check DFT connections

Key Features:

- DFT violation checking
- ATPG coverage estimation
- Test Robustness and Glitch Monitoring
- Test Points Selection
- Connectivity Validation (facilitates design agnostic custom methodology)

DFT Violation Checks

TestMAX Advisor can be used to check a design for DFT violations, and this provides an early insight into the testability problems, it also speeds up time to DFT and ensures that RTL is scan ready. Resolving at-speed test issues at the RTL can save weeks of effort. TestMAX Advisor identifies timing closure issues caused by at speed tests, which often achieve lower fault coverage than required even when full-scan is utilized, and the stuck-at coverage is high.

TestMAX Advisor also performs lint checking to ensure the RTL or netlist can achieve maximum ATPG coverage. The tool verifies that the design meets scan DRC requirements, providing detailed audit reports that help designers identify missing test constraints and make appropriate modifications to the design to address scan issues. It also verifies that a multi-voltage design complies with low-power DFT rules. For example, one type of check ensures that low-power constraints are compatible with scan test requirements; another type, applicable to netlists, verifies that scan chains do not cross voltage domains without level shifters.

ATPG Coverage Estimation

TestMAX Advisor provides the maximum achievable ATPG coverage estimate for the design, and reports the hierarchical coverage estimate for the sub blocks and hierarchies. This helps to determine whether the coverage goal can be achieved, and which blocks or hierarchies are contributing to coverage last for the entire design. One of the important features of TestMAX Advisor is ATPG coverage estimation. The tool provides consistent and repeatable correlation between RTL and ATPG test coverage. For Stuck-at TestMAX Advisor's coverage estimate correlates within 1% to the actual ATPG coverage. Whereas for transition delay, TestMAX Advisor's coverage estimate correlates within 5% to the actual ATPG coverage. These correlations are expected provided that the DFT constraints are aligned between TestMAX Advisor and ATPG.

Test Robustness and Reliability

Glitch detection is the process of identifying and preventing glitches in the register-transfer level (RTL). Glitches can be caused by a number of factors including asynchronous signal transitions, clock domain crossing (CDC), sequential logic and timing errors. Testability profiling assesses test robustness, the susceptibility of test patterns to electrical glitches and identifies RTL constructs that limit maximum stuck-at and transition fault coverage. Rule violations always reference the RTL so that designers know exactly where to make changes. To easily diagnose testability issues in the RTL, TestMAX Advisor provides an intuitive, integrated debug environment that enables cross-probing among views.

Test Point Selection

Some of the faults in the design are ATPG testable but difficult to test. TestMAX Advisor identifies hard-to-test areas in the design and reports an ordered list of test points that can be inserted at hard to control and observe points to improve test coverage and reduce pattern count. The test points identified by TestMAX Advisor can then be inserted by TestMAX DFT. To reduce area congestion, physically-aware test points are supported where physical information about the test points selected by TestMAX Advisor can be used by Design Compiler® NXT and Fusion Compiler™ (as shown in the Synopsys design flow in Figure 1 and Figure 2). Test points are grouped based on physical data, allowing one flop to be shared across multiple test points, resulting in significant area overhead reduction.

A fault is deemed hard-to-detect if it has a very low probability of detection in a test composed entirely of randomly generated patterns. TestMAX Advisor analyzes random pattern coverage to identify hard-to-detect faults and suggests changes to meet testability goals. The random pattern coverage estimation is displayed in a hierarchical fault browser. Designers can quickly zoom into the blocks that have significant low coverage and further analyze which portion of the design leads to poor coverage.

Connectivity Validation

TestMAX Advisor validates connectivity across hierarchies checking both paths and values. This validation not only applies for test logic added at SoC integration level but also for any logic not related to test. TestMAX Advisor addresses connectivity challenges such as back-to-back on-chip controllers (OCCs) that find no clock control connection. Examples of value checks include PLL resets or clock gating enable pins. Conditional checks are also supported, for example memory sleep controlled by pin at IP level. Connectivity validation can be performed either at RTL or gate-level netlists. Connectivity Checks can also be used to create design-agnostic custom methodologies.

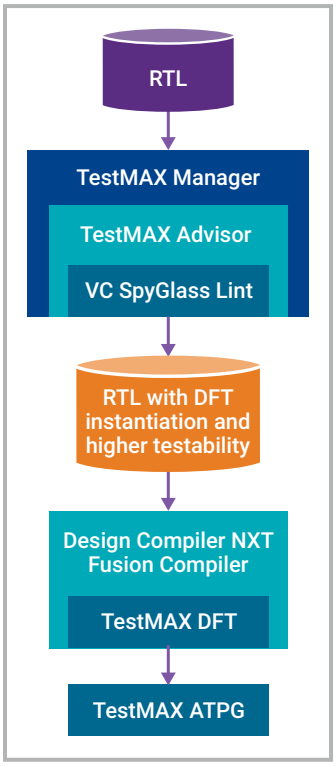

Figure 1: TestMAX Advisor addresses testability issues early in the design flow

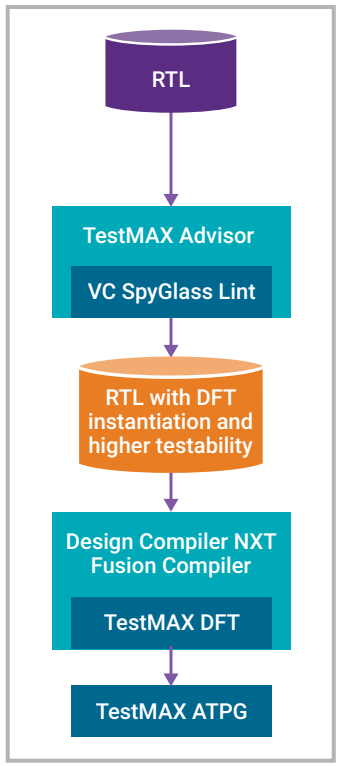

Figure 2: TestMAX Advisor in RTL creation flow

User Interface Example

The TestMAX Advisor Integrated debug environment enables cross-probing among views to easily diagnose testability issues

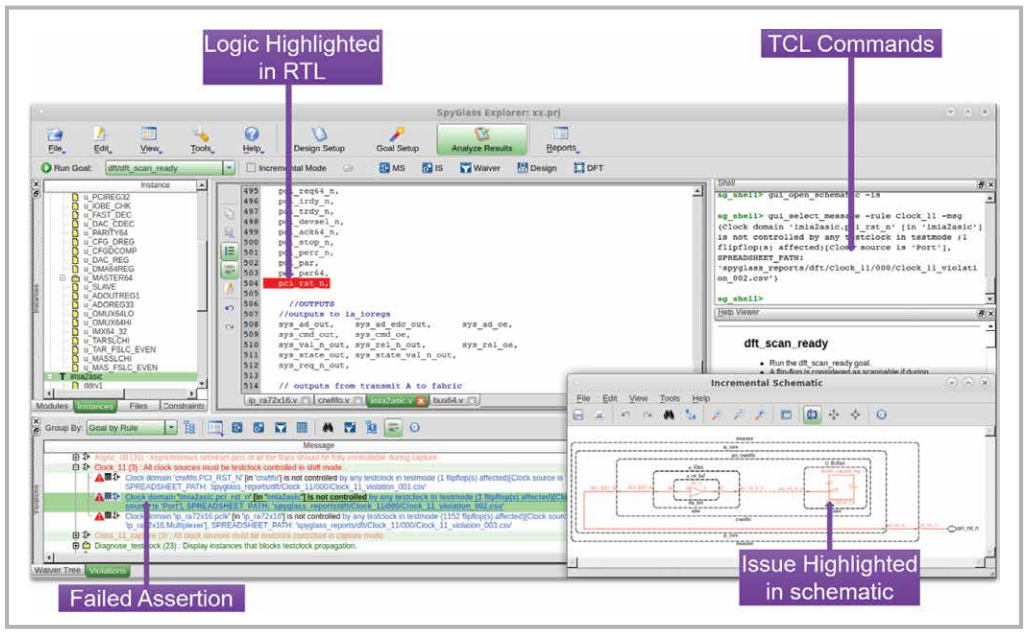

Figure 3: TestMAX Advisor debug environment

Reference Methodology

The TestMAX Advisor reference methodology provides a structured, easy-to-use, and comprehensive process for resolving RTL design issues, thereby ensuring high quality RTL with fewer design bugs. The methodology leads to fewer but more meaningful violations, thus saving time for the designer. The methodology documentation and rule sets are provided with TestMAX Advisor.

Design Formats

TestMAX Advisor supports the following data formats:

- Design: VHDL, Verilog (RTL or netlist), SystemVerilog
- Test Models: SPF/CTL
- Constraints: SDC and SpyGlass SGDC, Tcl
- Power: UPF
- Verification: VCD, FSDB

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