PrimePower RTL to Signoff Power Analysis

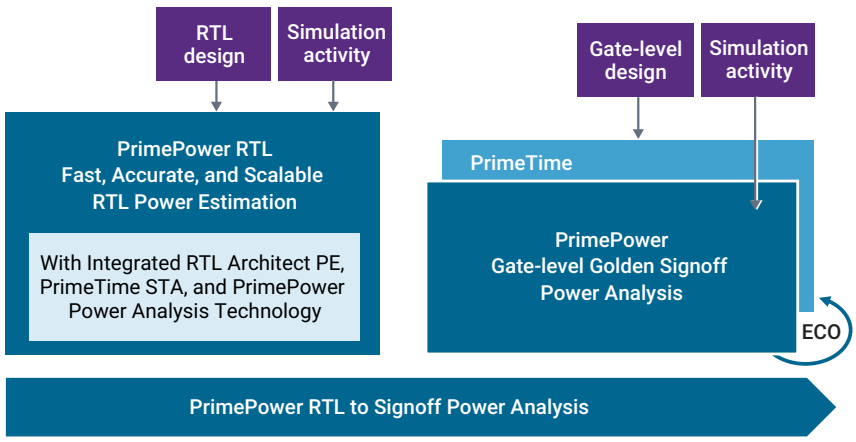
Delivering accurate dynamic and leakage power analysis from RTL to Signoff

Overview

The Synopsys PrimePower product family enables accurate power analysis for block-level and full-chip designs starting from RTL, through the different stages of implementation, and leading to power signoff.

PrimePower RTL power estimation provides RTL designers with fast, scalable, and accurate power estimation for early analysis of RTL blocks, subsystems, and full-SoCs. Supported power analysis includes average power, peak power, glitch power, clock network power, dynamic and leakage power, and multi-voltage power; with activity from RTL vectors from simulation, emulation, and vectorless analysis.

PrimePower RTL power estimation delivers strong correlation with implementation and signoff stage analysis through the direct integration of Synopsys' RTL Architect™ predictive engine (PE), PrimeTime® static timing analysis (STA), and PrimePower gate-level power analysis technologies. By providing early and accurate visibility into RTL power numbers, PrimePower RTL enables designers to analyze, explore, and optimize their RTL with confidence, improving power, energy efficiency, and shortening the design cycle.

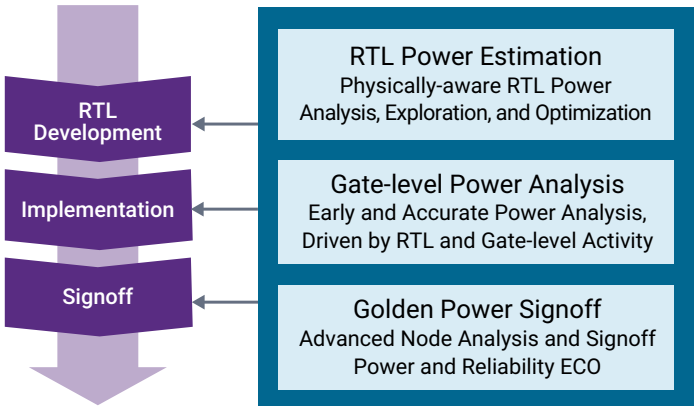


During implementation and signoff, PrimePower provides accurate gate-level power analysis reports for SoC designers to make timely design optimizations and achieve power targets. Supported power analysis includes average power, peak power, glitch power, clock network power, dynamic and leakage power, and multi-voltage power; with activity from RTL and gate-level vectors from simulation, emulation, and vectorless analysis.

By closely integrating with PrimeTime, the golden industry standard for timing and signal integrity analysis and signoff, PrimePower expands the PrimeTime solution to deliver accurate dynamic and leakage power analysis and signoff for gate-level designs.

PrimePower RTL to Signoff Power Analysis—Technology Highlights

The PrimePower RTL to Signoff Power Analysis solution provides SoC designers with accurate, signoff-consistent power estimation and analysis throughout the design implementation process.



RTL Power Estimation with PrimePower RTL

PrimePower RTL power estimation accurately predicts RTL power to enable fast what-if analysis, provide guidance to improve clock gating efficiency, memory access rate and data path power, and close on average and peak power budgets sooner.

- RTL vectors from simulation and emulation, and vectorless what-if analysis
- RTL average, peak, glitch, clock, dynamic, leakage, and multi-voltage power analysis & reporting
- Clock-gating, memory, data-path, and glitch power exploration and guidance
- Physically-aware, signoff-consistent power estimation results
- Graphical debug and waveform visualization

Gate-level Power Analysis and Golden Power Signoff with PrimePower

During gate-level implementation and signoff, PrimePower builds a detailed, timing-aware power profile of the design based on connectivity, switching activity, net capacitance, and cell-level power behavior data. Power consumption is analyzed and reported at the chip, block, and cell levels, including power maps and waveforms for visual power debug.

- Vectorless average and target power what-if analysis
- Concurrent reading of RTL and gate-level vectors from simulation and emulation
- Gate-level average, peak, glitch, clock, dynamic, leakage, and multi-voltage power analysis & reporting
- Early glitch analysis, peak power analysis, and IR profiling using PrimePower activity delay shifting
- Glitch-aware SAIF file generation for implementation power recovery and ECO signoff
- Efficient IPF, STA, & glitch-aware FSDB file generation for use in Ansys® RedHawk™ IR-drop analysis
- Advanced node analysis and signoff including Cell-EM, context-aware leakage, and CCS support
- Graphical debug and waveform visualization

For more information about PrimePower RTL to Signoff Power Analysis, contact your local Synopsys sales representative.

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