SYNOPSYS®

DATASHEET

IC Compiler II

Industry Leading Place and Route System

Accelerating Design Closure on Advanced Designs

Overview

IC Compiler™ II is the industry leading place and route solution that delivers best-in-class quality-of-results (QoR) for next-generation designs across all market verticals and process technologies while enabling unprecedented productivity. IC Compiler II includes innovative for flat and hierarchical design planning, early design exploration, congestion aware placement and optimization, clock tree synthesis, advanced node routing convergence, manufacturing compliance, and signoff closure.

IC Compiler II is specifically architected to address aggressive performance, power, area (PPA), and time-to-market pressures of leading-edge designs. Key technologies include a pervasively parallel optimization framework, multi-objective global placement, routing driven placement optimization, full flow Arc based concurrent clock and data optimization, total power optimization, multi-pattern and FinFET aware flow and machine learning (ML) driven optimization for fast and predictive design closure. Advanced Fusion technologies offer signoff IR drop driven optimization, PrimeTime® delay calculation within IC Compiler II, exhaustive path-based analysis (PBA) and signoff ECO within place and route for unmatched QoR and design convergence.

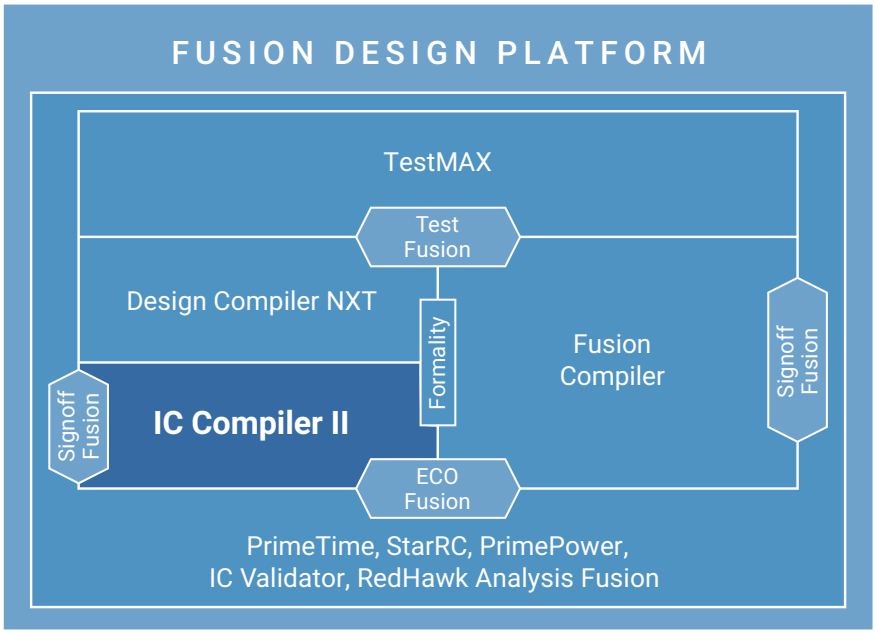

Figure 1: IC Compiler II Anchor in Synopsys Design Platform

Key Benefits

Productivity

- The highest capacity solution that supports 500M+ instances with a scalable and compact data model
- A full suite of design planning features including transparent hierarchical optimization
- Out-of-the-box simple reference methodology for easy setup
- Multi-threaded and distributed computing for all major flow steps
- Golden signoff accuracy with direct access to PrimeTime delay calculation

PPA

- Unified TNS driven optimization framework
- Congestion, timing, and power-driven logic re-synthesis
- IEEE 1801 UPF/multi-voltage support
- Arc-based concurrent clock and data optimization
- Global minima driven total power optimization

Advanced Nodes

- Multi-pattern and FinFET aware design flow
- Next generation advanced 2D placement and legalization
- Routing layer driven optimization, auto NDR, and via pillar optimization
- Machine learning driven congestion prediction and DRC closure
- Highest level of foundry support and certification for advanced process nodes
- IC Validator in the loop signoff driven DRC validation and fixing

Advanced Fusion Technology

- Physically aware logic re-synthesis
- IR drop driven optimization during all major flow steps
- PrimeTime delay calculation based routing optimization for golden accuracy
- Integrated PrimeTime ECO flow during routing optimization for fastest turnaround time

Empowering Design Across Diversified Applications

The dizzying pace of innovation and highly diversified applications across the design spectrum is forcing a complete rethink of the place and route systems to design and implement differentiated designs in a highly competitive semiconductor market on schedule. Designers on emerging process nodes must meet aggressive PPA and productivity goals. It essentially means efficient and intelligent handling of 100s of millions of place-able instances, multiple levels of hierarchy, 1000s of hard macros, 100s of clocks, wide busses, and 10s of modes and corners power domains and complex design constraints and process technology mandates.

Emphasis on Designer Productivity

IC Compiler II is architected from the ground up for speed and scalability. Its hierarchical data model consumes 2-3X less memory than conventional tools, boosting the limits of capacity to 500M placeable instances and beyond. Adaptive abstraction and on-the-fly data management minimize memory requirements and enable fast responsive data manipulation. Near-linear multi-core threading of key infrastructural components and core algorithms such as database access and timing analysis speed up optimization at all phases of design. Patented, lossless compact modeling and independent R and C extraction allow handling more modes and corners (MCMM scenarios) with minimal runtime impact.

IC Compiler II has built-in Reference Methodology(RM) that ensures fast flow bring up. This RM Flow is Foundry Process/Design Type specific to ensure a robust starting point and seamless bring up. IC Compiler II has direct access to the Golden PrimeTime delay calculation engine to minimize ECO iterations.

IC Compiler II's new data model enables designers to perform fast exploration and floorplanning with complex layout requirements. IC Compiler II can create bus structures, handle designs with n-levels of physical hierarchy, and support Multiply Instantiated Blocks (MIBs) in addition to global route driven pin assignment/feedthrough flow, timing driven macro placement, MV area design planning.

A design data mismatch inferencing engine analyzes the quality of inputs and drives construct creation on the fly, delivering design insights even with "incomplete" data early in the design cycle. Concurrent traversal of logical and physical data models enables hierarchical Data-Flow Analysis (DFA) and fast interactive analysis through multi-level design hierarchies and MIBs. Data flow and feedthrough paths highlighted in Figure 2 allow analysis and manipulation through n-levels of hierarchy to complete early design exploration and prototyping.

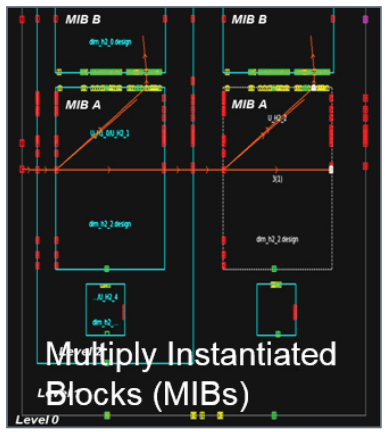

Figure 2: Fast interactive analysis through multiple-levels of physical hierarchy and MIB

Pipeline-register-planning shown in Figure 3, provides guidance for optimal placement to meet the stringent timing requirements of high-performance designs. Interactive route editor integrated which is advanced node aware shown in Figure 4, allows intricate editing and routing functions, including the creation of special signal routes, buses, etc.

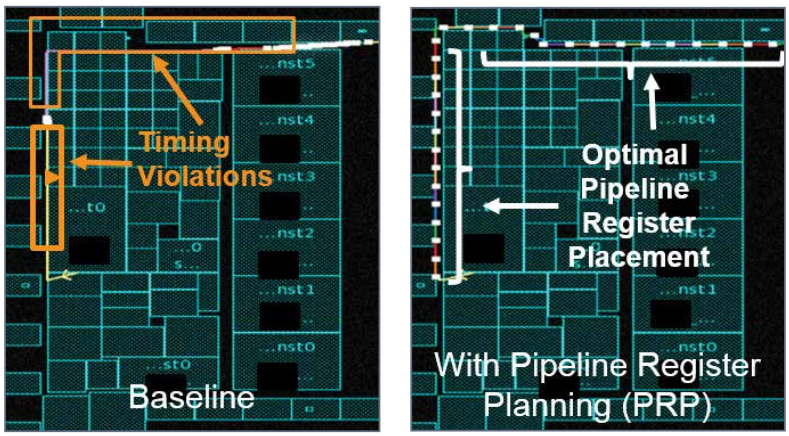

Figure 3: Pipeline register placement enables superior QoR for designs with complex buses

Achieving Best Performance, Power, Area, and TAT

IC Compiler II features a new optimization framework built on global analytics. This Unified TNS Driven Optimization framework is shared with Design Compiler NXT synthesis to enable physically-aware synthesis, layer assignment, and route-based optimization for improved PPA and TAT. Multi-Corner Multi-Mode (MCMM) and Multi-Voltage (MV) aware, level-based analytical algorithms continuously optimize using parallel heuristic algorithms. Multi-factor costing functions deliver faster results on both broad and targeted design goals. Concurrent PPA driven logic remapping, rewiring, and legalization interleaved with placement minimizes congested logic, resulting in simple localized logic cones that maximize routability and QoR.

IC Compiler II minimizes leakage with fast and efficient cell-by-cell power selection across HVT, SVT and LVT cells and varying channel lengths. Activity-driven power optimization uses VCD/ SAIF, net toggle rates, or probability functions to drive placement decisions and minimize pin capacitances. Multi-bit register banking optimizes clock tree structures, reduces area, and net length, while automatically managing clock, data, and scan chain connections.

Advanced modeling of congestion across all layers highlighted in Figure 4 provides accurate feedback throughput the flow from design planning to post- route optimization.

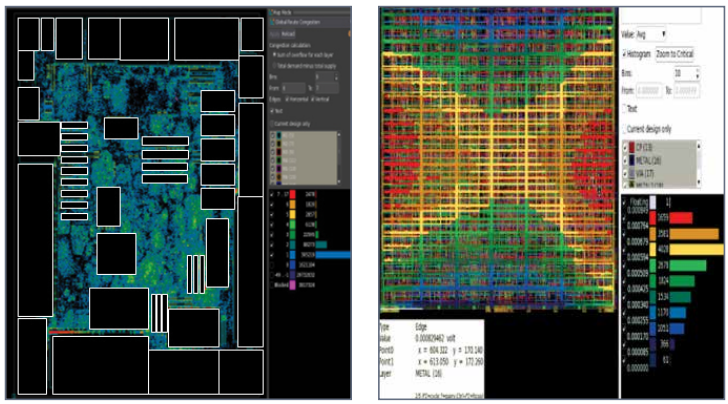

Figure 4: Intelligent and accurate analysis for congestion and power

IC Compiler II introduces a new Concurrent Clock and Data (CCD) analysis and optimization engine that is built-in to every flow step resulting in meeting both aggressive performance and minimizing total power footprint. ARC-based CCD optimization performs clock tree traversal across all modes/corners in path-based fashion to ensure optimal delay budgeting.

Robust support for clock distribution enables virtually any clock style, including mesh, multi-source, or H-tree topologies. Advanced analysis and debugging features perform accurate clock QoR analysis and debugging as highlighted in Figure 5.

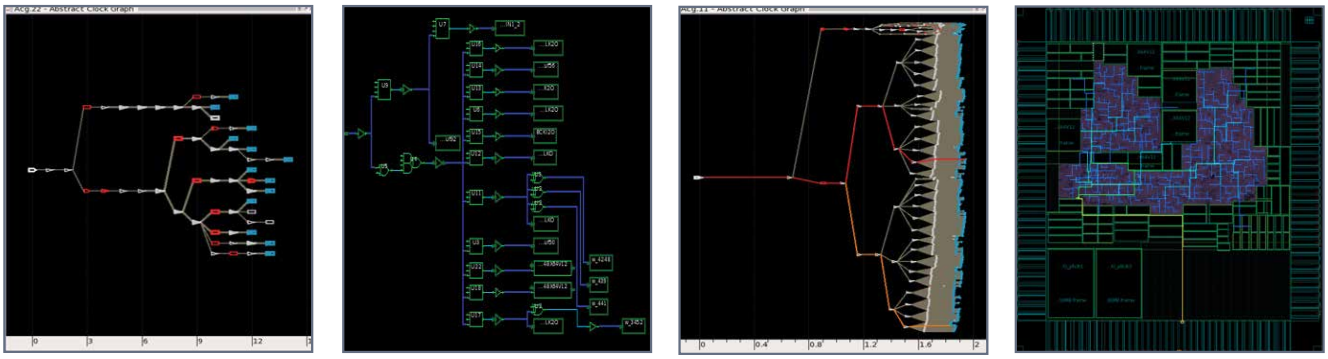

Figure 5: Accurate clock QoR analysis and debugging (a & b) Abstracted clock graph and schematic.
(c) Latency clock graph. (d) Colored clock tree in layout.

IC Compiler II features many innovative technologies that make it the ideal choice for high-performance, energy-efficient Arm® processor core implementation, resulting in industry-best milliwatts/megahertz (mW/MHz) for mobile and other applications across the board. Synopsys and Arm work closely together to offer optimized implementation of popular Arm cores for IC Compiler II, with reference flows available for Arm Cortex®-A high-performance processors and Mali GPUs. In addition, Arm offers off-the-shelf Artisan® standard cell and memory models that have been optimally tuned and tested for fast deployment in an IC Compiler II environment. Continuous technology innovation and close collaboration makes IC Compiler II the leading choice for Arm-based high-performance design.

Highest Level of Advanced Node Certification and Support

IC Compiler II provides advanced node design enablement across major foundries and technology nodes—including 16/14nm, 12/10nm, 7/5nm, and sub-5nm geometries. Zroute digital router technology ensures early and full compliance with the latest design rules required for these advanced node technologies. Synopsys collaborates closely with all the leading foundries to ensure that IC Compiler II is the first to deliver support for early prototype design rules and support for the final production design rules. IC Compiler II design technologies maximize the benefits of new process technologies and offer optimal return on investment for cutting-edge silicon applications.

IC Compiler II advanced node design support includes multi-pattern/FinFET aware placement and routing, Next-generation advanced 2D placement and legalization, routing layer driven optimization, auto NDR, and via pillar optimization. IC Validator in the loop provides signoff DRC feedback during Implementation.

Figure 6: IC Validator In-Design metal fill color aware metal fill, optimized for density and foundry requirements

Machine learning driven congestion prediction and DRC closure allow for fastest routing convergence with best PPA. Multiple sets of training data are used to extract key predictive elements that guide the pre-route flow.

Advanced Fusion Technology

The Fusion Design Platform™ delivers unprecedented full-flow QoR and time-to-results (TTR) to accelerate the next wave of semiconductor industry innovation. The industry's first AI-enhanced, cloud-ready Design Platform with Fusion Technology™ is built from Synopsys' market-leading, massively-parallel digital design tools, and augmented with innovative capabilities to tackle the escalating challenges in cloud computing, automotive, mobile, and IoT market segments and accelerate the next wave of industry innovation.

Fusion Technology redefines conventional EDA tool boundaries across synthesis, place-and-route, and signoff, sharing integrated engines across the industry's premier digital design products. It enables designers to accelerate the delivery of their next-generation designs with the industry-best QoR and the TTR.